CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An apparatus for sensing a logic state of a memory cell, comprising:

a control circuit providing a control signal to said memory cell, said control signal controlling when said memory cell is sensed;

a switching circuit that receives a cellplate count signal and a bit count signal provided by said control circuit, said switching circuit further receiving a cellplate line signal and a bit line signal from said memory cell, said switching circuit producing a first output signal and a second output signal, wherein one of said first output signal and said second output signal is at a supply voltage and the other of said first output signal and said second output signal alternates polarity with each sensing operation; and

a comparison circuit receiving said first and second output signals and outputting a signal corresponding to the logic state of said memory cell.

2. The apparatus according to claim 1, wherein said control circuit comprises:

a cellplate counter that produces said cellplate count signal;

a digit counter that produces said bit count signal; and

an exclusive-or (XOR) gate that produces said control signal.

3. The apparatus according to claim 2, wherein said control circuit comprises:

a first inverter for receiving said cellplate count and producing an inverted cellplate count signal and applying said inverted cellplate count signal to said switching circuit; and a second inverter for receiving said bit count signal and producing an inverted bit count signal and applying said inverted bit count signal to said switching circuit.

4. The apparatus according to claim 3, wherein said comparison circuit further comprises:

a third inverter for receiving said inverted cellplate count signal and producing an inverted signal;

a first multiplexer for receiving said inverted signal, said inverted cellplate count signal, said first output signal, and said second output signal, said first multiplexer producing a third output signal;

a second multiplexer for receiving said inverted signal, said inverted cellplate count signal, said first output signal, and said second output signal, said second multiplexer producing a fourth output signal; and

a switched capacitor sensing amplifier for selecting one of said first output signal and said second output signal, said selected one of said first output signal and said second output signal corresponding to said logic state of said memory cell.

5. The apparatus according to claim 1, wherein said comparison circuit comprises a switched capacitor sensing amplifier for selecting one of said first output signal and said second output signal, said selected one of said first output signal and said second output signal corresponding to the logic state of said memory cell.

6. The apparatus according to claim 1, wherein said switching circuit comprises:

a first inverter for receiving said cellplate count and producing an inverted cellplate count signal and applying said inverted cellplate count signal to said switching circuit;

a second inverter for receiving said bit count signal and producing an inverted bit count signal and applying said inverted bit count signal to said switching circuit.

a third inverter for receiving said inverted cellplate count signal and producing an inverted signal;

a first multiplexer for receiving said inverted signal, said inverted cellplate count signal, said first output signal, and said second output signal, said first multiplexer producing a third output signal; and

a second multiplexer for receiving said inverted signal, said inverted cellplate count signal, said first output signal, and said second output signal, said second multiplexer producing a fourth output signal.

7. A resistive memory cell comprising:

a memory element having at least two resistive states; and

a first connection and a second connection to first and second sensing lines respectively, said memory element being connected in series between said first connection and said second connection and capable of conducting sensing current alternately from said first sensing line to said second sensing line and from said second sensing line to said first sensing line.

8. The resistive memory cell according to claim 7, wherein said memory element is a programmable contact random access memory (PCRAM) element.

9. The resistive memory cell according to claim 7, further comprising a switching element connected in series with said memory element that controls sensing of said memory element.

10. A sensing circuit for resistive memory cells, comprising:

first and second sensing lines between which are connected a memory element having at least two resistive memory states;

switching circuitry that provides sensing current through the memory element alternately from said first sensing line to said second sensing line and from said second sensing line to said first sensing line; and

output circuitry that receives said sensing current and, in response, provides an output signal indicating a resistance state of said memory element.

11. A memory device comprising:

an array of memory cells;

a cellplate line common across said array of memory cells; and

an apparatus for sensing a logic state of one of said memory cells, said apparatus comprising:

first and second sensing lines between which are connected to a memory element having at least two resistive memory states;

switching circuitry that provides sensing current through the memory element alternately from said first sensing line to said second sensing line and from said second sensing line to said first sensing line; and

output circuitry that receives said sensing current and, in response, provides an output signal indicating a resistance state of said memory element.

12. A processing system, comprising:

a processor; and

a memory device coupled to said processor via a bus, said memory device comprising:

an array of memory cells,

a cellplate line common across said array of memory cells, and

an apparatus for sensing a logic state of one of said memory cells, said apparatus comprising:

first and second sensing lines between which are connected a memory element having at least two resistive memory states;

switching circuitry that provides sensing current through the memory element alternately from said first sensing line to said second sensing line and from said second sensing line to said first sensing line; and

output circuitry that receives said sensing current and, in response, provides an output signal indicating a resistance state of said memory element.

13. An integrated circuit comprising:

a memory device, said memory device comprising:

an array of memory cells,

a cellplate line common across said array of memory cells, and

an apparatus for sensing a logic state of one of said memory cells, said apparatus comprising:

first and second sensing lines between which are connected a memory element having at least two resistive memory states;

switching circuitry that provides sensing current through the memory element alternately from said first sensing line to said second sensing line and from said second sensing line to said first sensing line; and output circuitry that receives said sensing current and, in response, provides an output signal indicating a resistance state of said memory element.

14. A method of sensing a resistive state of a resistive memory element, said method comprising:

providing sensing current alternately in a first direction and a second opposite direction through said memory element; and

in response to said sensing current, providing an output signal indicating a resistance state of said memory element.

15. A method for sensing a logic state of a memory cell, said method comprising:

receiving a clock signal from a clock source;

producing a cellplate count signal;

producing an inverted cellplate count signal;

applying said cellplate count signal, said inverted cellplate count signal, a first signal based on a cellplate line of said memory cell, a second signal based on a bit line of said memory cell to a comparison circuit to produce a signal corresponding to said logic state of said memory cell.

16. The method according to claim 15, further comprising:

producing a bit count signal; and

producing a control signal based on said cellplate count and said digit count, said control signal applied to said memory cell to control when sensing occurs.

17. The method according to claim 16, further comprising:

producing an inverted bit count signal;

applying said inverted cellplate count signal to a gate of a first transistor, said first transistor coupled to said cellplate line of said memory cell;

applying said inverted bit count signal to a gate of a second transistor, said second transistor coupled to said bit line of said memory cell;

producing said first signal; and

producing said second signal.

18. A processing system, comprising:

a processor; and

a memory device coupled to said processor via a bus, said memory device comprising:

an array of memory cells,

a cellplate line common across said array of memory cells, and

an apparatus for sensing a logic state of a memory cell, comprising:

a control circuit providing a control signal, said control signal controlling when said memory cell is sensed;

a switching circuit that receives a cellplate count signal and a bit count signal provided by said control circuit, said switching circuit further receiving a cellplate line signal and a bit line signal from said memory cell, said switching circuit producing a first output signal and a second output signal, wherein one of said first output signal and said second output signal is at a supply voltage and the other of said first output signal and said second output signal alternates polarity with each sensing operation; and

a comparison circuit receiving said first and second output signals and outputting a signal corresponding to the logic state of said memory cell.